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January 8, 2000

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 09/729,152 12/04/00

M.S. Lin

HIGH PERFORMANCE SUB-SYSTEM DESIGN AND ASSEMBLY

Grp. Art Unit: 2825

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,534,465 to Frye et al., "Method for Making Multichip Circuits using Active Semiconductor Substrates", discloses a method for fabricating a chip-on-chip structure which has a first chip connected to a second chip with a solder bump.

U.S. Patent 5,481,205 to Frye et al., "Temporary Connections for Fast Electrical Access to Electronic Devices", describes a structure of making temporary connections of chips having solder bumps or ball-grid array.

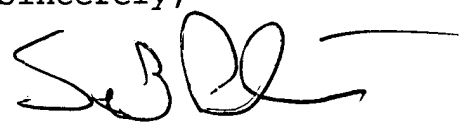
The following two U.S. Patents teach a method for fabricating programmable ESD protection circuits for multichip semiconductor structures:

1) U.S. Patent 5,731,945 to Bertin et al., "Multichip Semiconductor Structures with Consolidated Circuitry and Programmable ESD Protection for Input/Output Nodes".
2) U.S. Patent 5,807,791 to Bertin et al., "Methods for Fabricating Multichip Semiconductor Structures with Consolidated Circuitry and Programmable ESD Protection for Input/Output Nodes".

U.S. Patent 5,461,333 to Condon et al., "Multi-Chip Modules having Chip-To-Chip Interconnections with Reduced Signal Voltage Level and Swing", shows a differential input/output buffer circuit for communicating small signal voltage levels between chips on a multi-chip module.

U.S. Patent 5,818,748 to Bertin et al., "Chip Function Separation Onto Separate Stacked Chips", illistrates a separation of chip function onto separate integrated circuits chips. This allows the optimization of the circuits.

Sincerely,



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